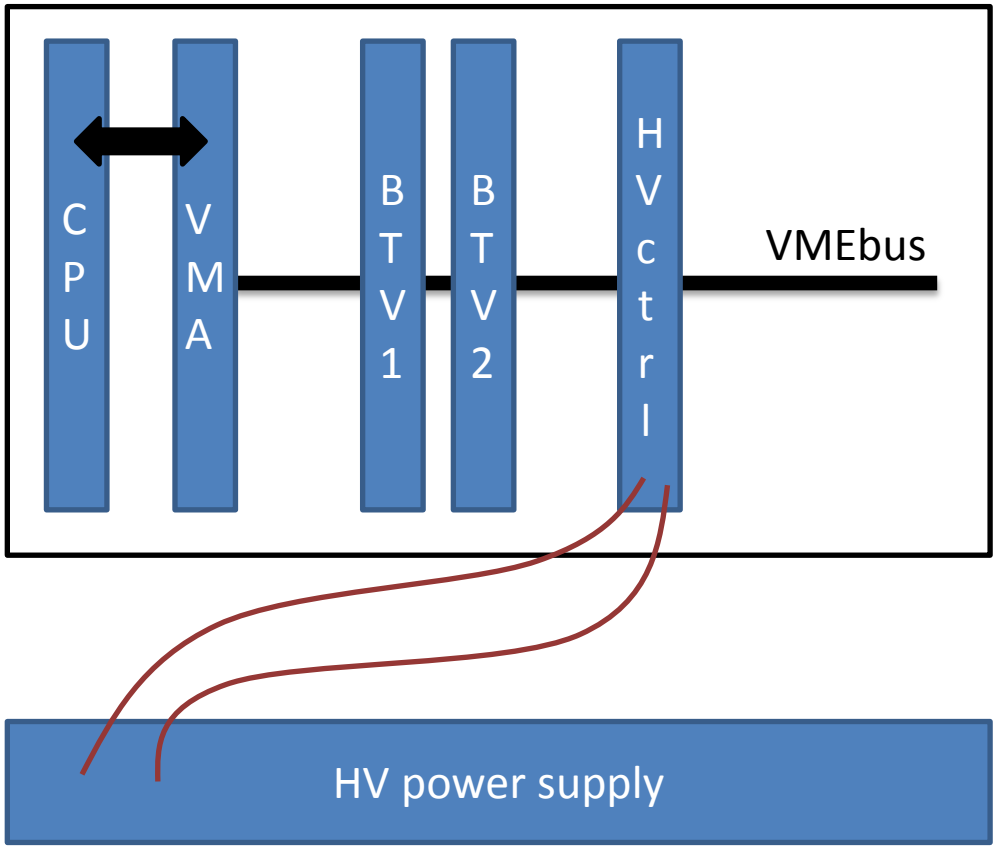
HVcontrol card debugging

Oliver Keller – 19.11.2013

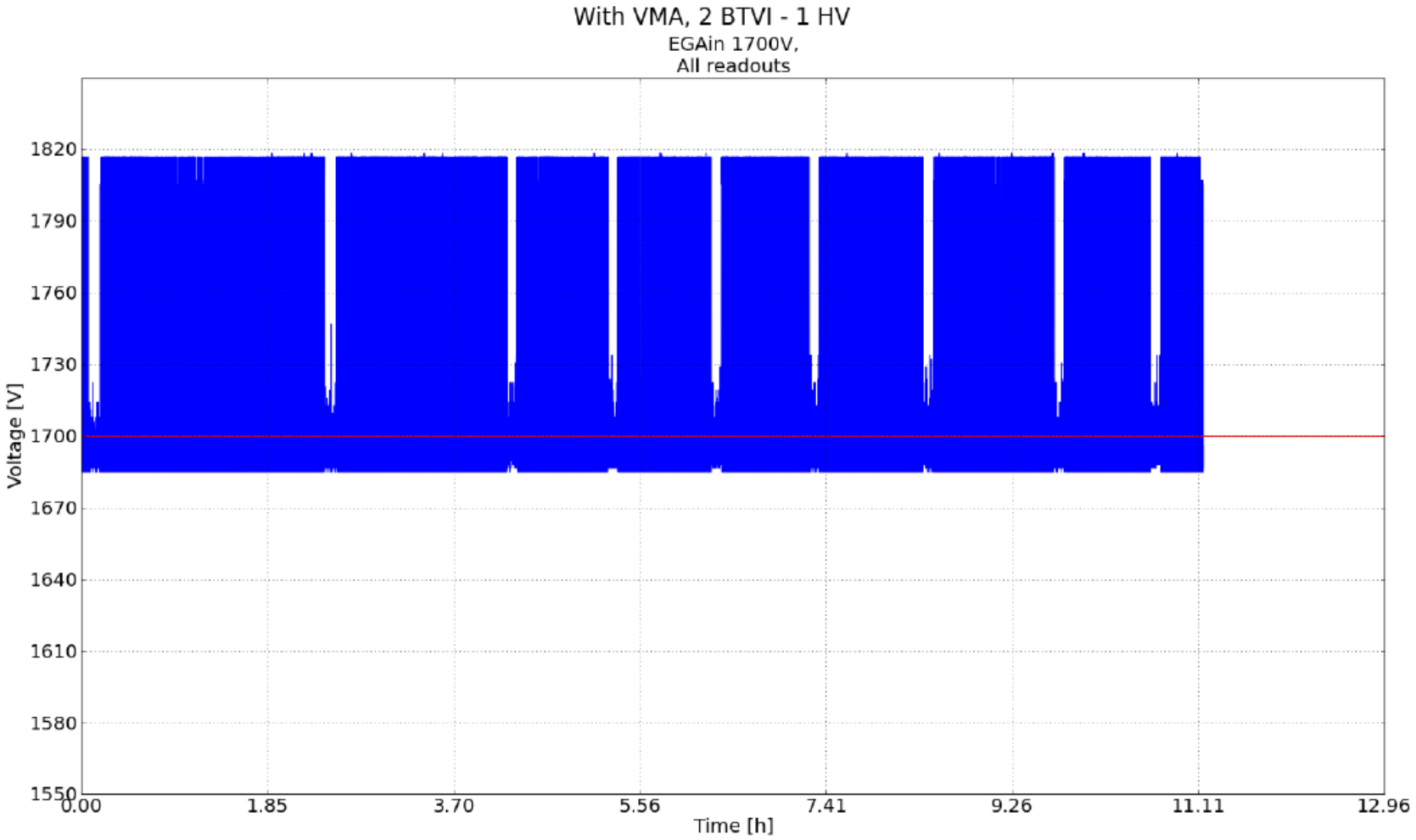
System Overview



HV control card:
4 general commands:
- Set DAC values
- Select ADC channel
- Trigger ADC conversion
- Read ADC channel

HV power supply:
Only analog electronics
- EMCO HV modules
- Voltage and current measurement circuits
- Over-voltage range selection

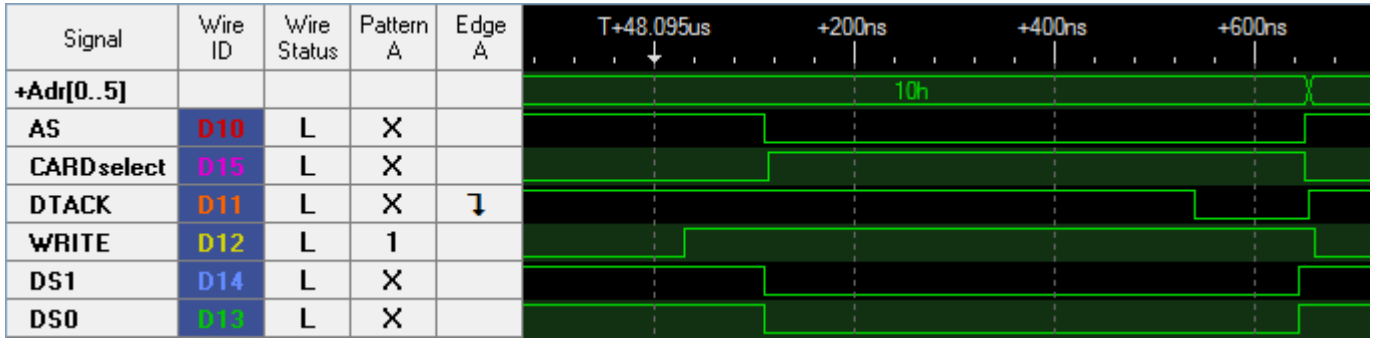
Previous Test Results



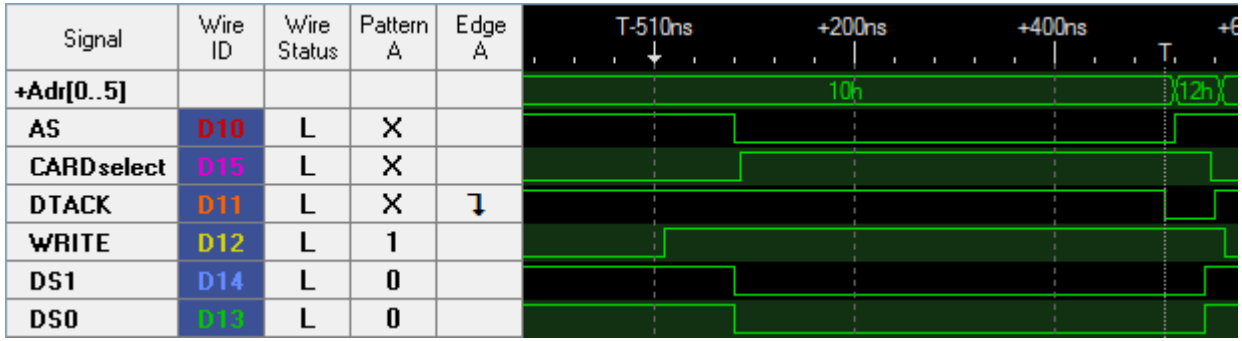
Logic Analyser Debugging

With/Without VMA

With VMA



Without VMA



Difference:
With VMA adressess are not changed during the cycle, only after DS0/1=high
But Intel card behaviour is completely valid (address pipelining)

Reasons

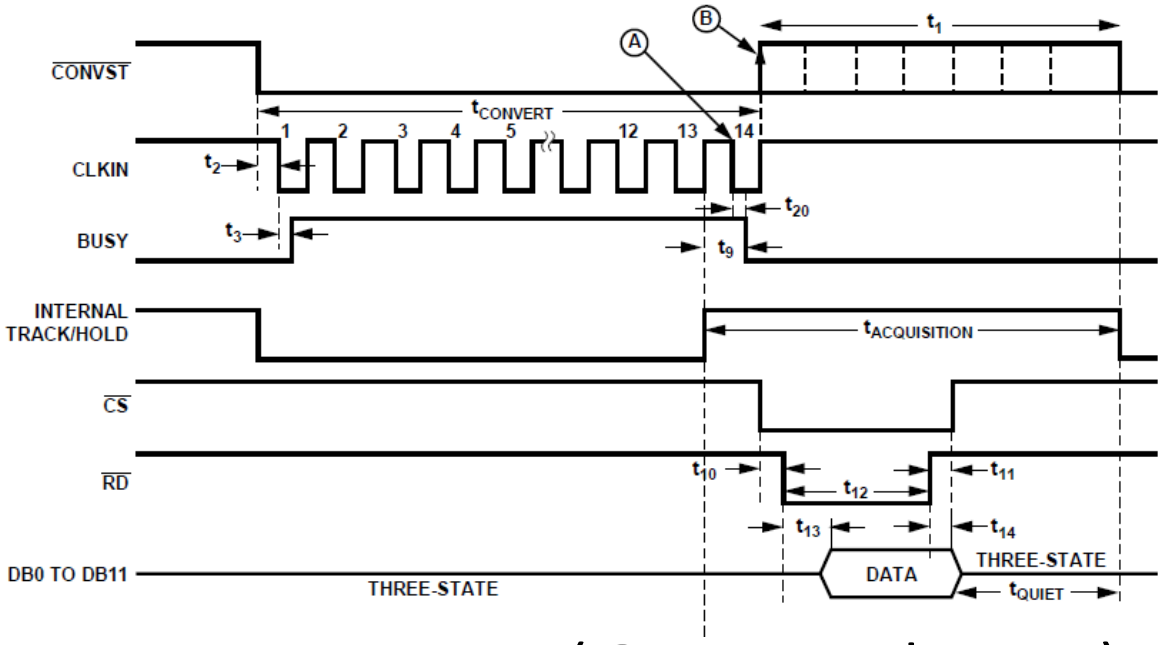
- No latching of anything on the card (in or out)
- Address is verified constantly while AS signal is ignored
- Simple logic equations control the bus access:

```
!cs_i = a23 & (a22 !$ !b22)
            & (a21 !$ !b21)
            & (a20 !$ !b20)
            & (a19 !$ !b19)
cs = !cs_i & (amx==^h39) & !ds0 & !ds1
ds = !(!cs_i & (amx==^h39) & !ds0 & !ds1)

add = [a5,a4,a3,a2,a1,0]
conv  macro {!(cs & (add==50) & !w)}
Convst_ADC1  = !(!(conv & !(!Convst_ADC1 & busy_ADC1)))
!ADC1_cs = cs & ((add>=16) & (add<=30))
!rb = cs & ((add>=0) & (add<=46)) & w
```

ADC conversion delay

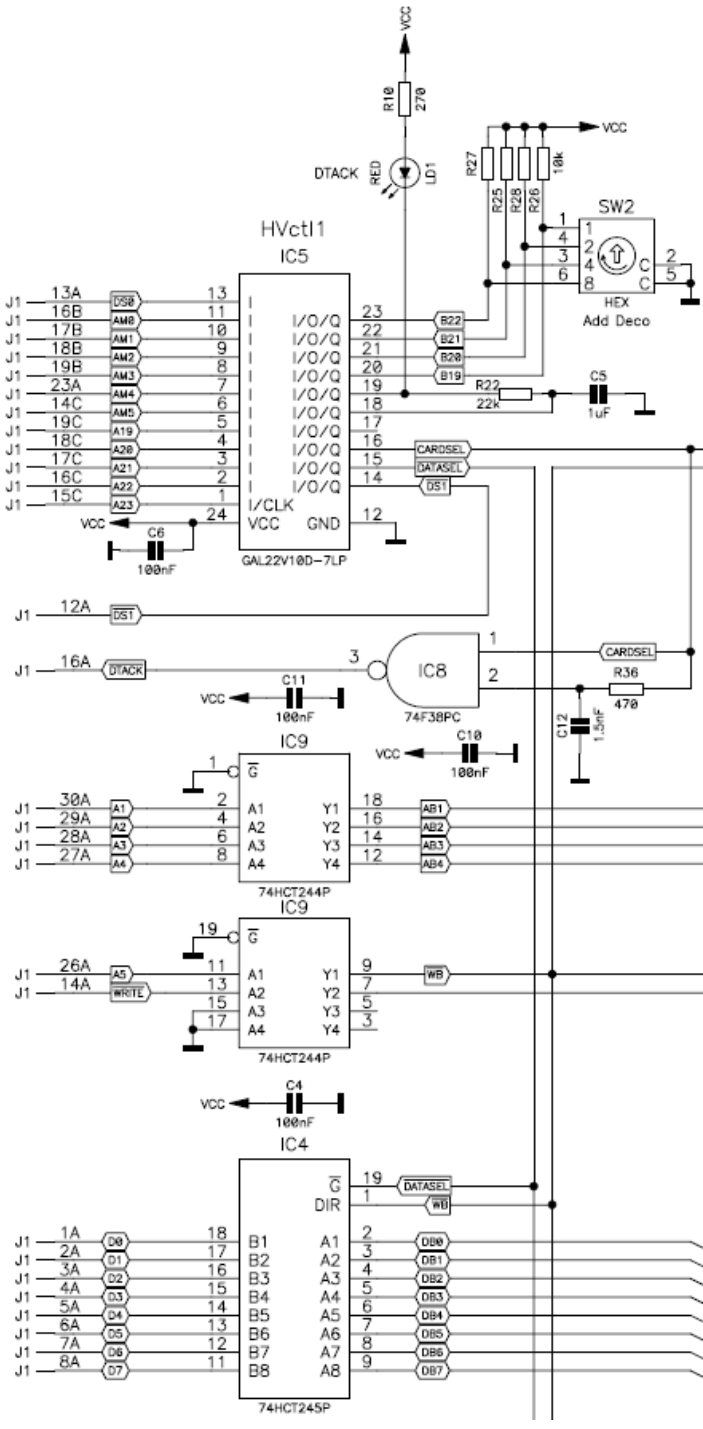
- AD7938, 8 channel, 10 Bit ADC. 12 MHz clock



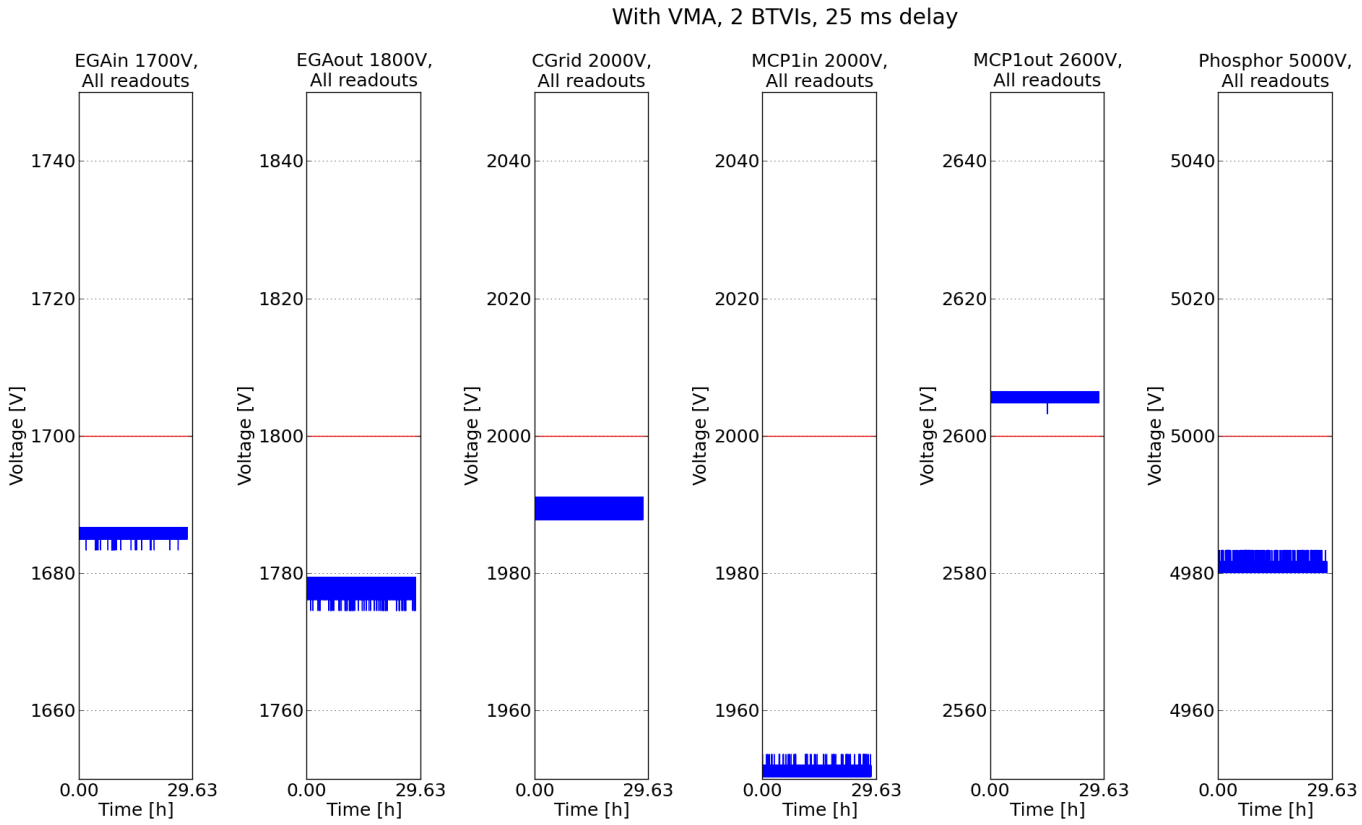
- T_convert = 1.125us (@ 12 sample MHz)
- T_aquisition = 125ns

VMEbus access

- Fixed setting of DTACK low after ~430ns when C12 is charged
- ADC conversion still in progress when VME cycle has already finished
- Delay between VME commands must reflect ADC conversion time requirements
- Delay between other commands must ensure ADC channel readout is finished before next channel selection (write to ADC) happens
- Save suggestion: at least 2us delay between all commands

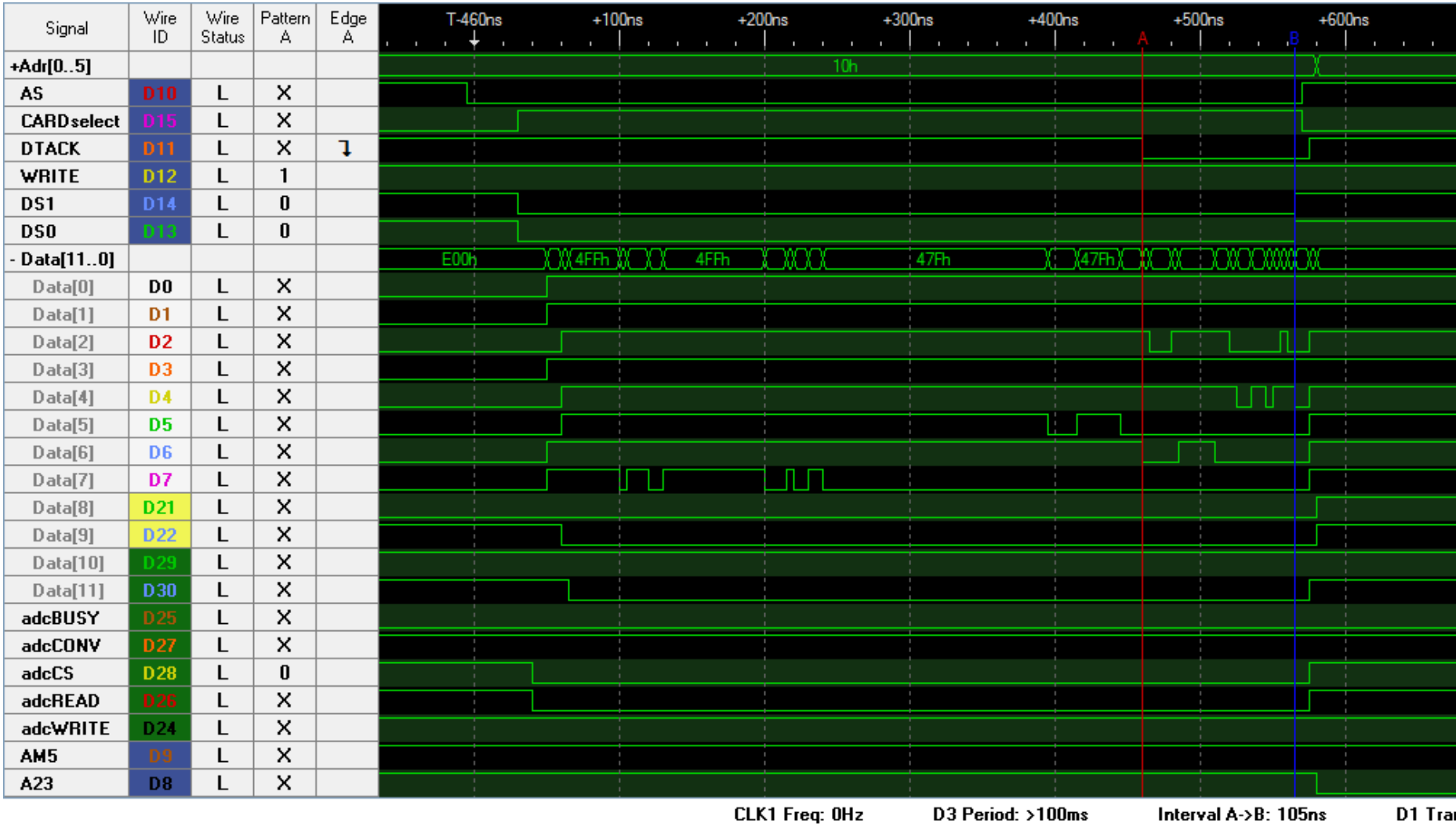


Test with additional delays



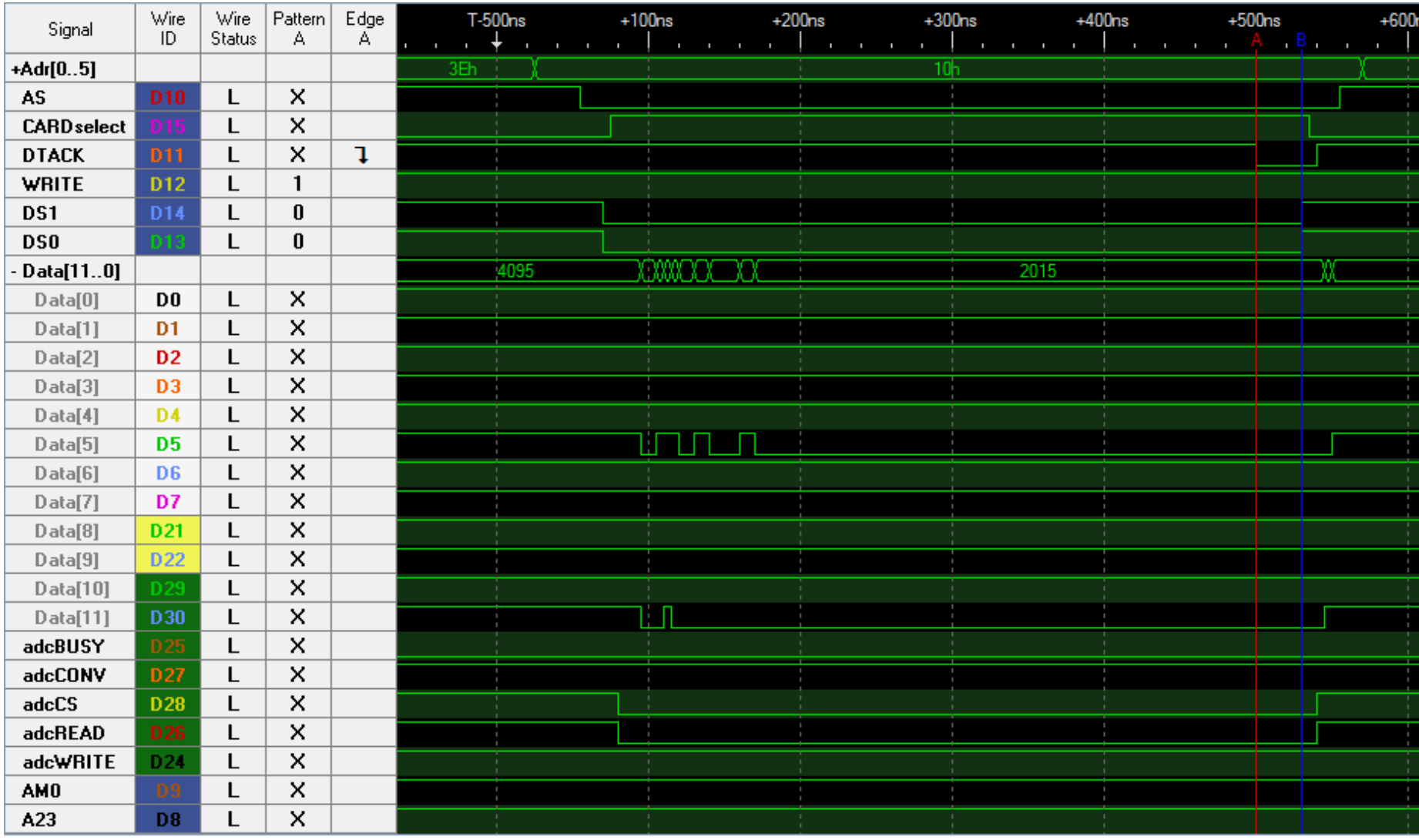
Corresponds to about 1 Hz readout of all channels/ports

Looking at the data lines



No difference with or w/o VMA here.

Comparison with PPC



Clean driven data lines.

Summary

- HV control card is not compatible to address pipelining on VME bus, should latch the address form the bus during address strobe cycle
- Intel card is sending VME commands at a much higher rate than the old PPC card
- High level software must ensure proper timing/delays on the VMEbus to be compatible to this card => bad idea
- Adding of 10uF capacitors (ceramic X7R) on ADCs, GALs and line driver power supplies did not make any difference regarding data line signal stability
- PPC and Intel card's VME bus line driver circuits seem to differ
  => check data signal lines before line driver on HV ctrl. card with a scope